

## CLAIMS

What is claimed is:

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- 1 1. A microelectronic package, comprising:
  - 2 a heat sink;
  - 3 at least one microelectronic die having an active surface and a back surface, said
  - 4 at least one microelectronic die back surface adjacent to said heat sink; and
  - 5 an encapsulation material disposed on said heat sink and said microelectronic die
  - 6 active surface.

- 1 2. The microelectronic package of claim 1, further including a build-up layer
- 2 disposed on an upper surface of said encapsulation material.

- 1 3. The microelectronic package of claim 2, wherein said build-up layer
- 2 comprises at least one conductive trace disposed on said encapsulation material upper
- 3 surface, wherein a portion of said at least one conductive trace extending through said
- 4 encapsulation material to contact said at least one microelectronic die active surface.

- 1 4. The microelectronic package of claim 3, wherein said build-up layer
- 2 further includes at least one dielectric layer disposed on at least a portion of the
- 3 encapsulation material upper surface and said at least one conductive trace, and at least
- 4 one second conductive trace extending through said at least one dielectric layer to contact
- 5 said at least one conductive trace.

1        ~~5.        The microelectronic package of claim 1, further including a thermally~~  
2        ~~conductive adhesive layer disposed between said at least one microelectronic die and said~~  
3        ~~heat sink.~~

1            6.        A method of fabricating a microelectronic package, comprising:  
2            providing a heat sink;  
3            disposing a back surface of at least one microelectronic die adjacent to said heat  
4        sink;  
5            disposing an encapsulation material on said at least one microelectronic die and  
6        said heat sink.

1            7.        The method of claim 6, further including forming a build-up layer on an  
2        upper surface of said encapsulation material.

1            8.        The method of claim 7, wherein forming said build-up layer comprises  
2        forming at least one via from said encapsulation material upper surface to said at least  
3        one microelectronic die active surface and disposing at least one conductive trace on said  
4        encapsulation material upper surface, wherein a portion of said at least one conductive  
5        trace extending through said at least one via to contact said at least one microelectronic  
6        die active surface.

1           9.       The method of claim 8, further including disposing at least one dielectric  
2   layer on at least a portion of the encapsulation material upper surface and said at least one  
3   conductive trace, forming a via through said dielectric layer, and forming at least one  
4   second conductive trace on said dielectric layer, wherein a portion thereof extends  
5   through said at least one dielectric layer to contact said at least one conductive trace.

1           10.     A microelectronic package, comprising:  
2       a heat sink;  
3       a microelectronic package core having a first surface and an opposing second  
4   surface, said microelectronic package core having at least one opening defined therein  
5   extending from said microelectronic package core first surface to said microelectronic  
6   package core second surface, where said microelectronic package core second surface  
7   abuts said heat sink;  
8       at least one microelectronic die disposed within said at least one microelectronic  
9   package core opening and adjacent said heat sink, said at least one microelectronic die  
10   having an active surface; and  
11       an encapsulation material disposed on said microelectronic die and in portions of  
12   at least one microelectronic package core opening.

1           11.     The microelectronic package of claim 10, further including a build-up  
2   layer disposed on an upper surface of said encapsulation material.

1           12.     The microelectronic package of claim 11, wherein said build-up layer  
2 comprises at least one conductive trace disposed on said encapsulation material upper  
3 surface, wherein a portion of said at least one conductive trace extends through said  
4 encapsulation material to contact said at least one microelectronic die active surface.

1           13.     The microelectronic package of claim 12, wherein said build-up layer  
2 further includes at least one dielectric layer disposed on at least a portion of the  
3 encapsulation material upper surface and said at least one conductive trace, and at least  
4 one second conductive trace extending through said at least one dielectric layer to contact  
5 said at least one conductive trace.

1           14.     The microelectronic package of claim 11, wherein said encapsulation  
2 material covers said microelectronic package core first surface.

1           15.     The microelectronic package of claim 10, wherein a thickness of said  
2 microelectronic package core is greater than a thickness of said at least one  
3 microelectronic die.

1           16.     The microelectronic package of claim 10, wherein said microelectronic  
2 package core is a material selected from the group consisting of bismaleimide triazine  
3 resin based material, an FR4 material, polyimides, ceramics, and metals.

1           17.     The microelectronic package of claim 10, further including a thermally  
2     conductive adhesive layer disposed between said at least one microelectronic die and said  
3     heat sink.

1           18.     A method of fabricating a microelectronic package, comprising:  
2             providing a heat sink;  
3             disposing a back surface of at least one microelectronic die adjacent to said heat  
4     sink;  
5             abutting a microelectronic package core adjacent said heat sink, said  
6     microelectronic package core having at least one opening defined therein extending from  
7     a first surface of said microelectronic package core to a second surface of said  
8     microelectronic package core, said at least one microelectronic die residing within said at  
9     least one microelectronic package opening;  
10            disposing an encapsulation material on said at least one microelectronic die and in  
11     portions of at least one microelectronic package core opening.

1           19.     The method of claim 18, further including forming a build-up layer on an  
2     upper surface of said encapsulation material.

1           20.     The method of claim 19, wherein forming said build-up layer comprises  
2     forming at least one via from said encapsulation material upper surface to said at least  
3     one microelectronic die active surface and disposing at least one conductive trace on said

4 encapsulation material upper surface, wherein a portion of said at least one conductive  
5 trace extending through said at least one via to contact said microelectronic die active  
6 surface.

1 21. The method of claim 20, further including disposing at least one dielectric  
2 layer on at least a portion of the encapsulation material upper surface and said at least one  
3 conductive trace, forming a via through said dielectric layer, and forming at least one  
4 second conductive trace on said dielectric layer, wherein a portion thereof extends  
5 through said at least one dielectric layer to contact said at least one conductive trace.

1 22. The method of claim 18, wherein disposing said encapsulation material on  
2 said at least one microelectronic die and in portions of at least one microelectronic  
3 package core opening comprises disposing said encapsulation material on said at least  
4 one microelectronic die, in portions of at least one microelectronic package core opening,  
5 and said microelectronic package core first surface.

1 23. The method of claim 22, wherein abutting a microelectronic package core  
2 adjacent said heat sink comprises abutting a microelectronic package core, which is  
3 thicker than said at least one microelectronic die, adjacent said heat sink.

1 24. The method of claim 23, wherein disposing said encapsulation material on  
2 said at least one microelectronic die and in portions of at least one microelectronic

3 package core opening comprises disposing said encapsulation material on said at least  
4 one microelectronic die, in portions of at least one microelectronic package core opening,  
5 and said microelectronic package core first surface.

1 25. The method of claim 24, further including removing a portion of said  
2 encapsulation material on said microelectronic package core forming a uniform thickness  
3 of encapsulation material on said at least one microelectronic die.

1 26. The method of claim 25, further including forming a build-up layer on an  
2 upper surface of said encapsulation material.

1 27. The method of claim 26, wherein forming said build-up layer comprises  
2 forming at least one via from said encapsulation material upper surface to said at least  
3 one microelectronic die active surface and disposing at least one conductive trace on said  
4 encapsulation material upper surface, wherein a portion of said at least one conductive  
5 trace extending through said at least one via to contact said microelectronic die active  
6 surface.

1 28. The method of claim 27, further including disposing at least one dielectric  
2 layer on at least a portion of the encapsulation material upper surface and said at least one  
3 conductive trace, forming a via through said dielectric layer, and forming at least one

- 4 second conductive trace on said dielectric layer, wherein a portion thereof extends
- 5 through said at least one dielectric layer to contact said at least one conductive trace.

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